


# NB6306A

## Intel ADL-N Platform

### V3.0

01--COVER PAGE	31--LPDDR5 (DECAPS)	61--BLANK	91--Debug conn
02--Content	32--BLANK	62--BLANK	92--BLANK
03--BLOCK DIAGRAM	33--BLANK	63--BLANK	93--BLANK
04--PWR Sequence (1/2)	34--BLANK	64--BLANK	94--BLANK
05--PWR Sequence (2/2)	35--BLANK	65--BLANK	95--BLANK
06--SMBUS Control Table	36--BLANK	66--TypeC Controller_TPS65992D	96--BLANK
07--BOM Control Table	37--BLANK	67--BLANK	97--BLANK
08--ADL-N (MEMORY CHANNEL-A)	38--BLANK	68--BLANK	98--BLANK
09--BLANK	39--BLANK	69--BLANK	99--BUCK BOOST DUAL CHARGER
10--ADL-N (DISPLAY)	40--BLANK	70--TYPE C Connector_1	100--OWER DELIVERY V3P3A
11--ADL-N (CPU MISC/STRAP)	41--BLANK	71--BLANK	101--POWER DELIVERY V5P0A
12--ADL-N (PCIE/USB/SATA)	42--BLANK	72--BLANK	102--POWER DELIVERY V1P8A
13--ADL-N (CSI2, CNVI)	43--EC IT5571	73--BLANK	103--POWER VCCANA
14--ADL-N (SPI/ESPI/SMBUS/CLK)	44--EDP/CCD	74--BLANK	104--POWER VNN 1P05V
15--ADL-N (AUDIO/HDA/I2S)	45--MIPI CONN	75--BLANK	105--POWER DELIVERY VCCIN_AUX
16--ADL-N (I2C/ISH/UART/GPIO)	46--BLANK	76--BLANK	106--POWER DELIVERY IMVP
17--ADL-N (PWR MANAGEMENT)	47--HDMI 2.1 (PS8209)	77--BLANK	107--POWER DELIVERY VDDQ
18--ADL-N (CFG/RSVD)	48--BLANK	78--BLANK	108--POWER DC IN
19--ADL-N CPU POWER	49--AUDIO Codec ALC256	79--G sensor & HALL sensor	109--POWER DELIVERY LOADSWITCH
20--BLANK	50--BLANK	80--BLANK	
21--ADL-N PCH POWER	51--BLANK	81--TPM 2.0	
22--ADL-N (GND)	52--BLANK	82--Finger Print	
23--ADL-N (DECOUPLING1)	53--SYSTEM SPI FLASH ROM	83--BLANK	
24--ADL-N (DECOUPLING2)	54--SSD1 & SSD2	84--KeyBoard & KB BL & TP	
25--BLANK	55--EMMC	85--Thermal Sensor/FAN	
26--LPDDR5_CHA_1	56--UFS	86--Logic Circuit/ RTC/Stylus	
27--LPDDR5_CHA_2	57--USBA 3.2 GEN1 5G	87--BLANK	
28--BLANK	58--BLANK	88--IO/B&LTE&RJ45 Conn	
29--BLANK	59--CNVI & PCIE WLAN 2230	89--BLANK	
30--BLANK	60--BLANK	90--BLANK	

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## Content

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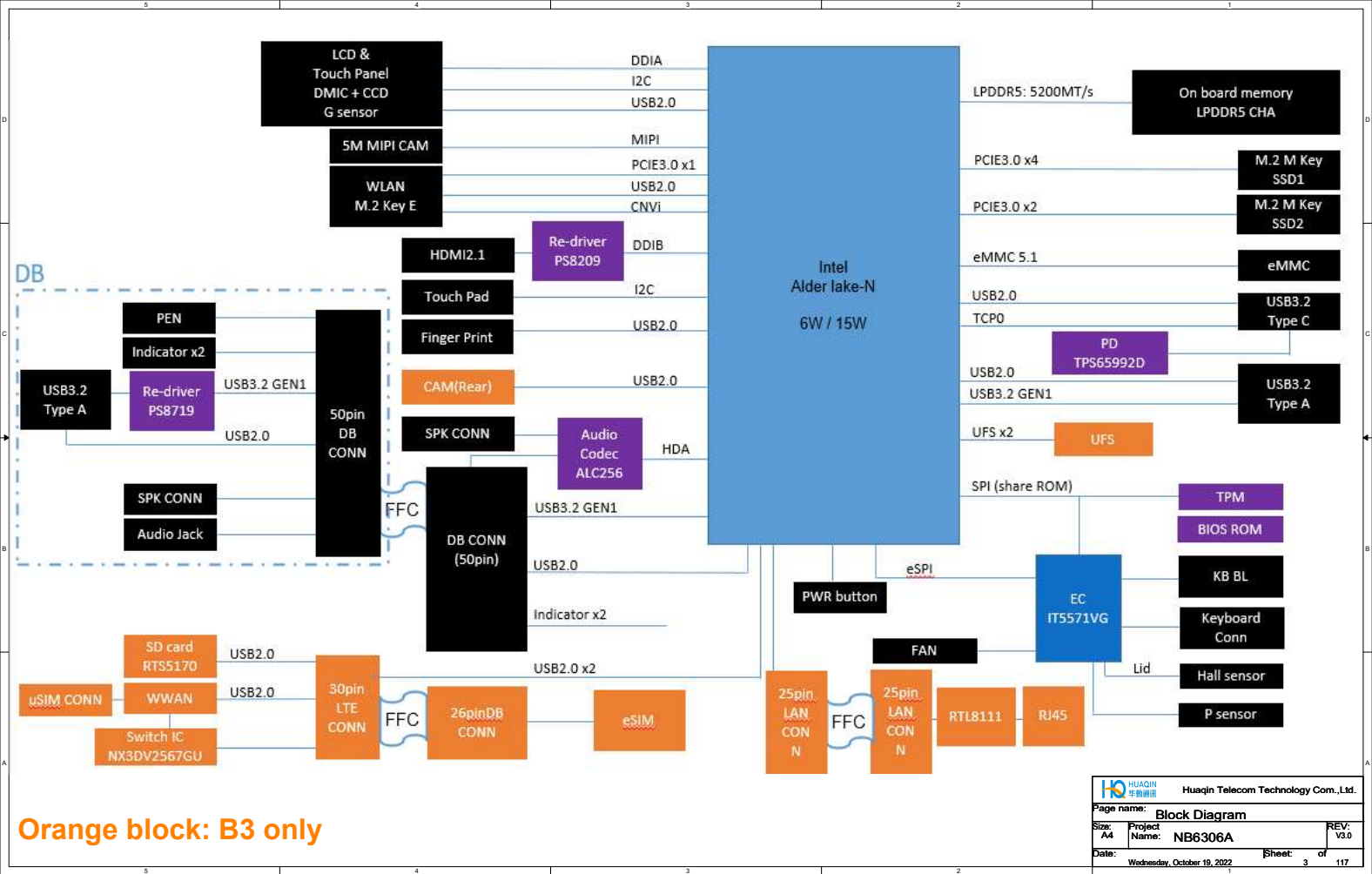
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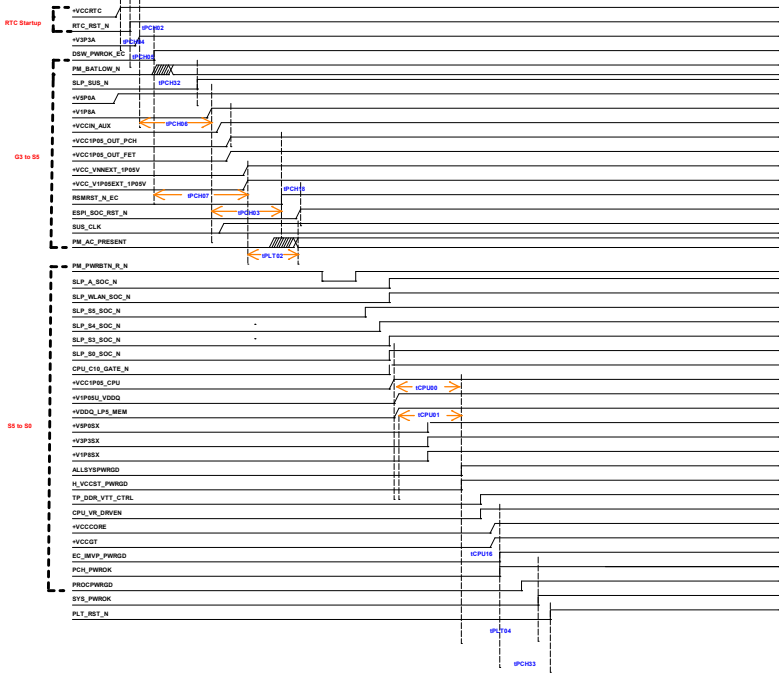
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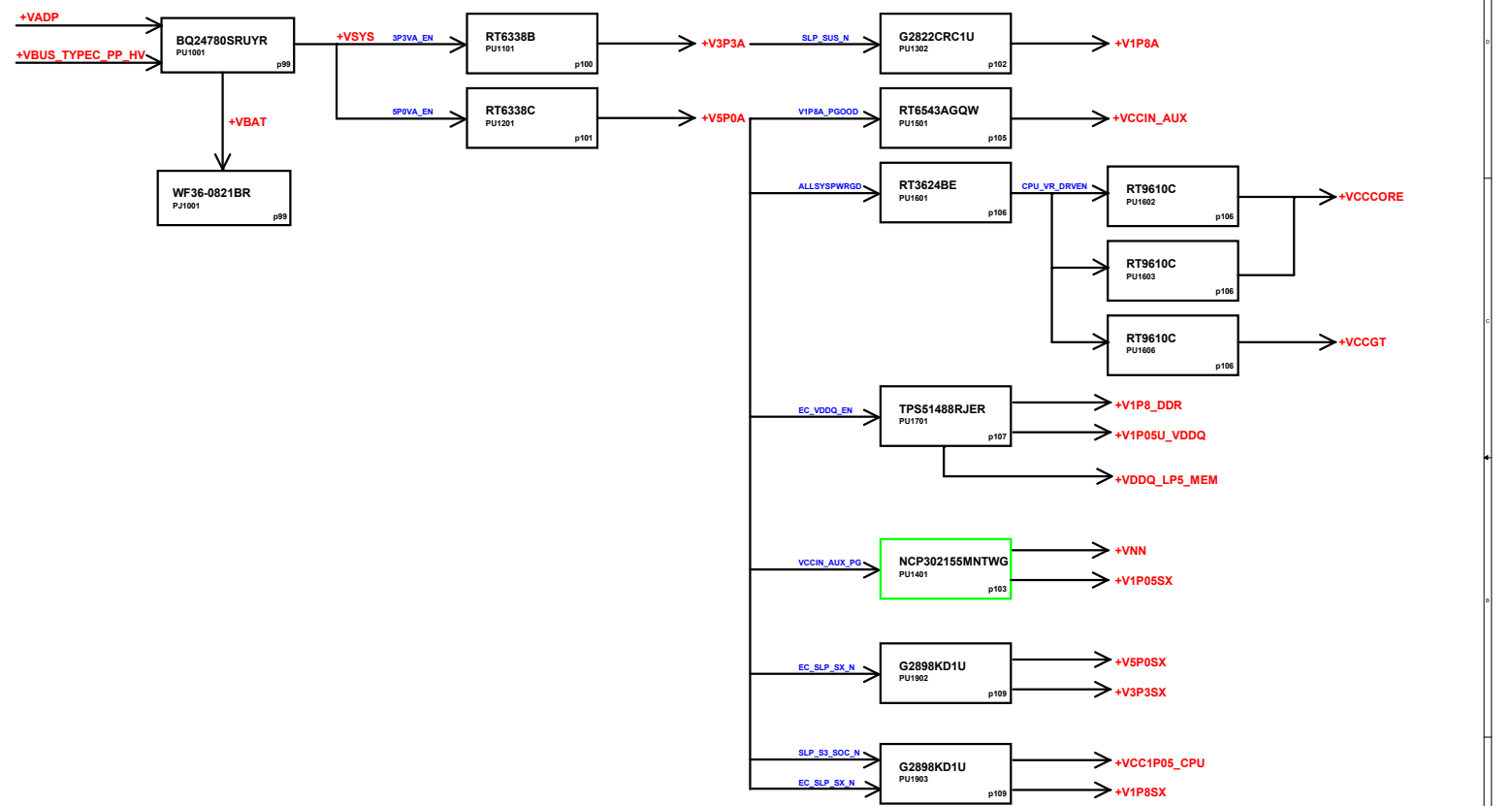
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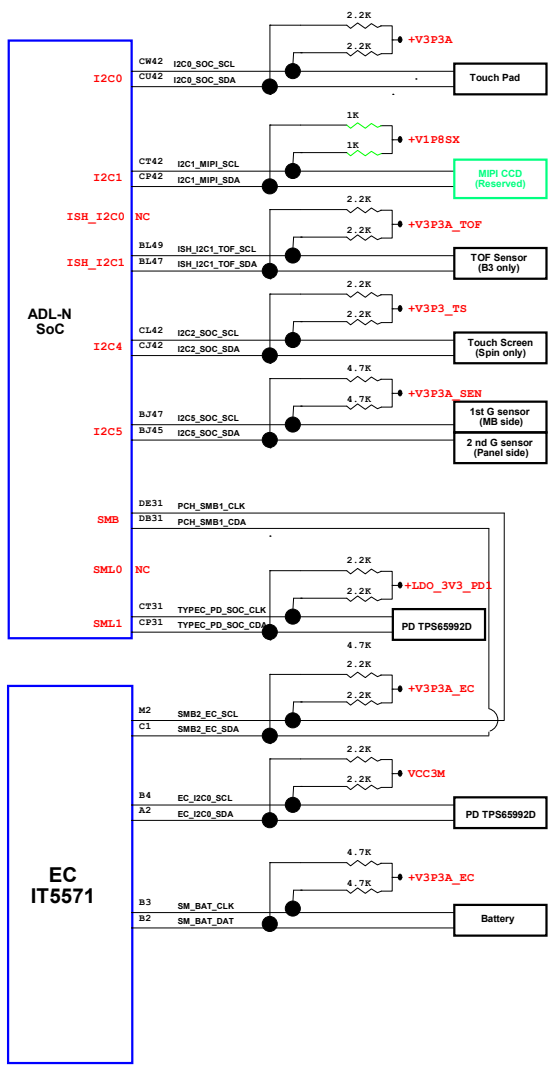


tCPU26	All	CPU	PLT	10	65	us	11	CPU_C10_GATE# de-assertion to VCSTG stable Note: CPU_C10_GATE# de-assertion to VCSTG also needs to meet max G5us on cold boot
tCPU27	All	CPU	PLT	10	240	us	11	CPU_C10_GATE# de-assertion to VCCL0 stable
tCPU33	All	CPU	PLT		240	us	11	CPU_C10_GATE# de-assertion to VCPLL0C stable

Item	Measure Point		Spec	NBS31A time	Result
SPCH01	HYOCRT	To	RTC REF N	128.5ms	PASS
SPCH04	HYOCRT	To	DSW PAROK EC		
SPCH05	RTC REF N	To	DSW PAROK EC		
SPCH06	HYOCRT	To	DSW PAROK EC		
SPCH08	DSW PAROK	To	SLP SUE N		
SPCH09	VYPRM PGDGO	To	VYPRM		
SPCH10	SSABST	To	RTC SOC REF N		
SPCH07	DSW PAROK EC	To	SSABST N EC		
SPCH03	VYPRM PGDGO	To	SSABST N EC		
SPCH12	SSABST N EC	To	SSABST N EC		
SPCH11	VYPRM PGDGO	To	VYPRM PGDGO	22ms	
ICPU00	HYOCRT CPU	To	VYPRM PGDGO		
ICPU01	HYOCRT CPU	To	VYPRM PGDGO		
ICPU02	HYOCRT CPU	To	VYPRM PGDGO		
ICPU03	HYOCRT CPU	To	VYPRM PGDGO		
ICPU04	HYOCRT CPU	To	VYPRM PGDGO	0.000ms	
ICPU05	HYOCRT CPU	To	VYPRM PGDGO		
ICPU06	HYOCRT CPU	To	VYPRM PGDGO	0.000ms	

Power Tree







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### BOM Control Table

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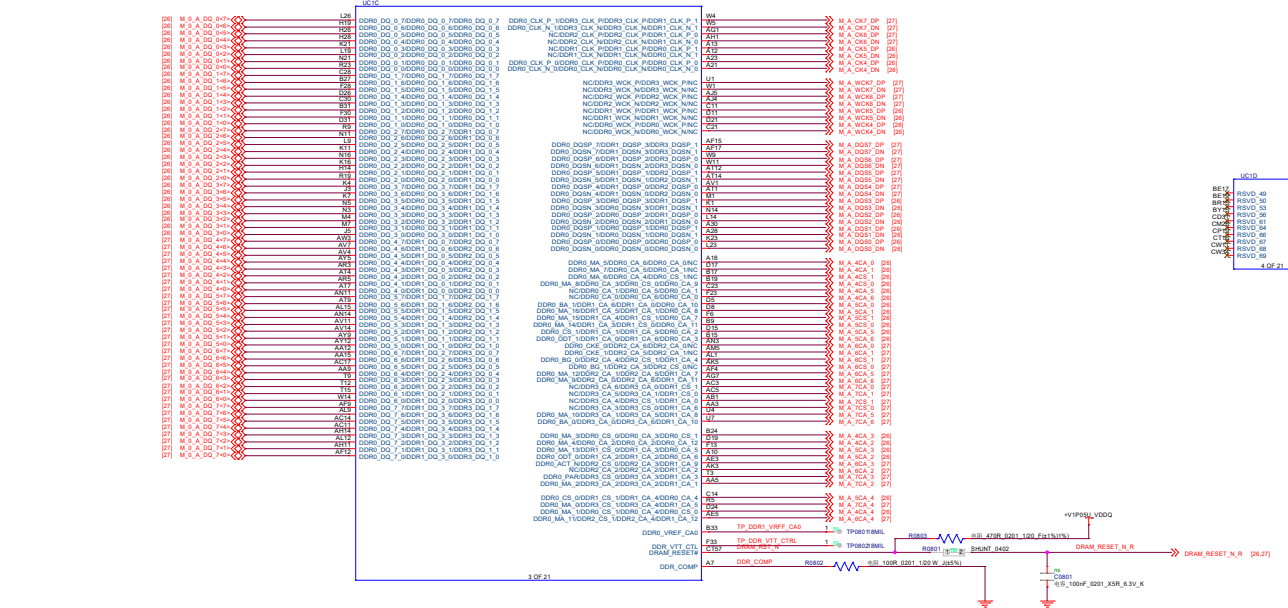
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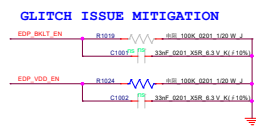
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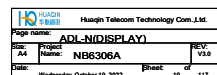
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**DNX CIRCUIT**

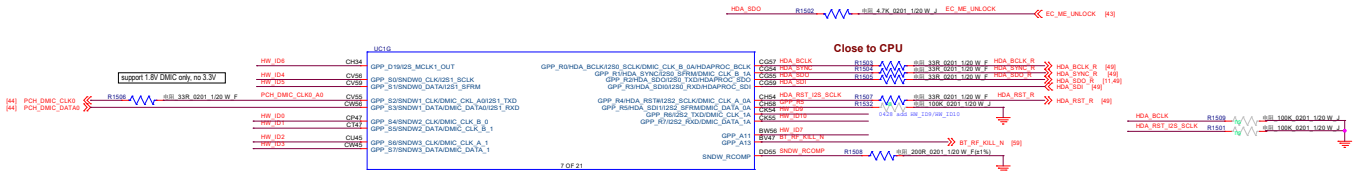




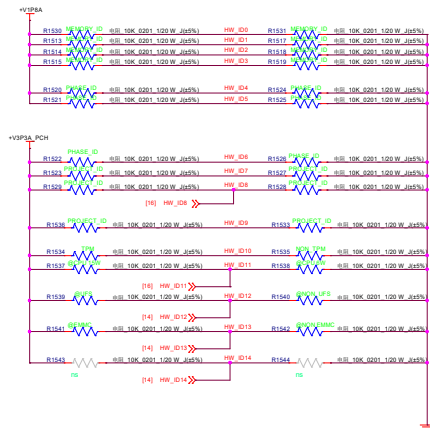








HDA_SYNC	C1501	0.0 20F 0201 RES/NR 25 V C08250
HDA_SCLK	C1502	0.0 20F 0201 RES/NR 25 V C08250
HDA_SDO	C1503	0.0 20F 0201 RES/NR 25 V C08250
HDA_RST_US_SCLK	C1508	0.0 20F 0201 RES/NR 25 V C08250
HDA_SDI	C1512	0.0 20F 0201 RES/NR 25 V C08250
PCH_DMC_CLK0	C1504	0.0 20F 0201 C08 40 V J
PCH_DMC_DATA0	C1505	0.0 20F 0201 C08 40 V J



Phase ID

HW_ID4	HW_ID5	HW_ID4	Description
0	0	0	PHY
0	1	0	PHY
1	0	0	PHY
1	1	0	NO
1	0	1	Reserved
1	1	0	Reserved
1	1	1	Reserved
0	0	0	Reserved

TPM ID

HW_ID10	TPM
0	0/1
1	NO TPM

UFS ID

UFS ID	UFS
0	W/O UFS
1	W/ UFS

EMMC ID

EMMC ID	EMMC
0	W/O EMMC
1	W/ EMMC

KB\_BL ID Reserved KB\_BL ID n#

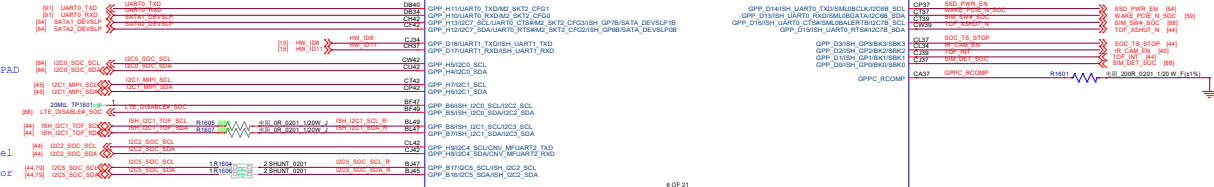
KB_BL ID	KB_BL
0	W/O KB_BL
1	W/ KB_BL

Project ID

HW_ID7	HW_ID8	HW_ID9	Description
0	0	0	NB6306A_15"
0	1	0	NB6306A_14"
1	0	0	NB6306A_13"
0	1	1	NB6306A_14" spin
1	0	1	NB6306A_14" 6W
1	1	0	Reserved
1	1	1	Reserved
0	0	0	Reserved

MEM ID

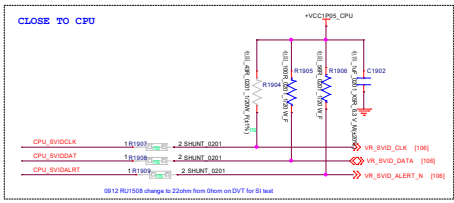
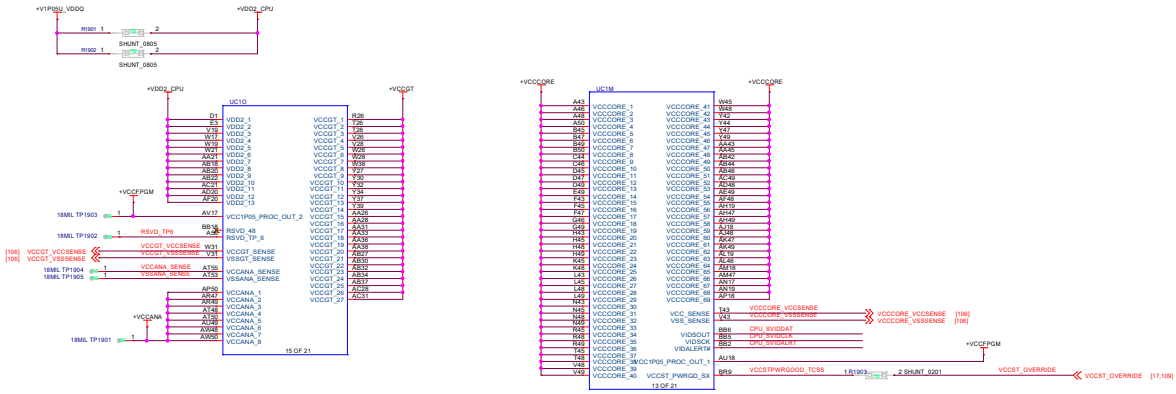
HW_ID10	HW_ID11	HW_ID12	HW_ID13	Description
0	0	0	0	MICRON LPDDR5 6400 3GB MT41FSD3208B-031 WT.B LP4VP V31M
1	0	0	0	HYUNDAI LPDDR5 6400 3GB H5V2808K3ML1R-W6 LP4VP DA
0	1	0	0	SAMSUNG LPDDR5 5500 3GB K3LAL08DM-MC0N LP4VP 1y
0	0	1	0	MICRON LPDDR5 6400 4GB MT41FSD3208B-031 WT.B LP4VP V31M
0	0	0	1	SAMSUNG LPDDR5 6400 4GB K3LAL08DM-MC0P LP4VP DA
1	1	0	0	HYUNDAI LPDDR5 6400 4GB H5V2808K3ML1R-W6 LP4VP DA
1	0	1	0	MICRON LPDDR5 6400 8GB MT41FSD3208B-031 WT.B LP4VP V31M
0	0	0	1	SAMSUNG LPDDR5 6400 8GB K3LAL08DM-MC0P LP4VP DA
0	1	1	0	HYUNDAI LPDDR5 6400 8GB H5V2808K3ML1R-W6 LP4VP DA
0	0	1	1	Reserved













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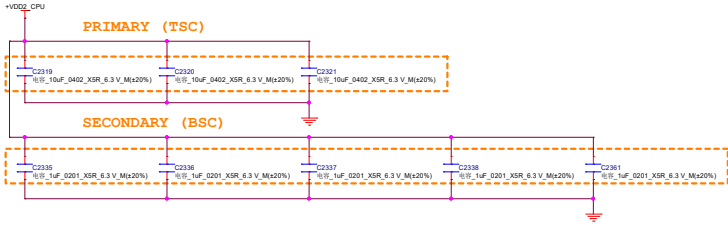




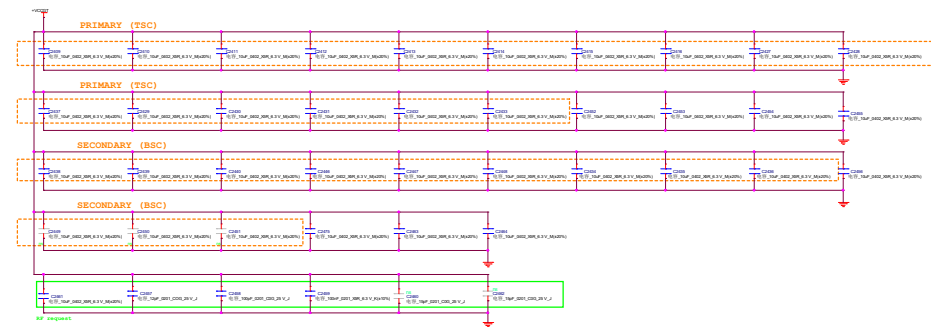
+VCCCORE



+VDD2\_CPU



## +VCCGT







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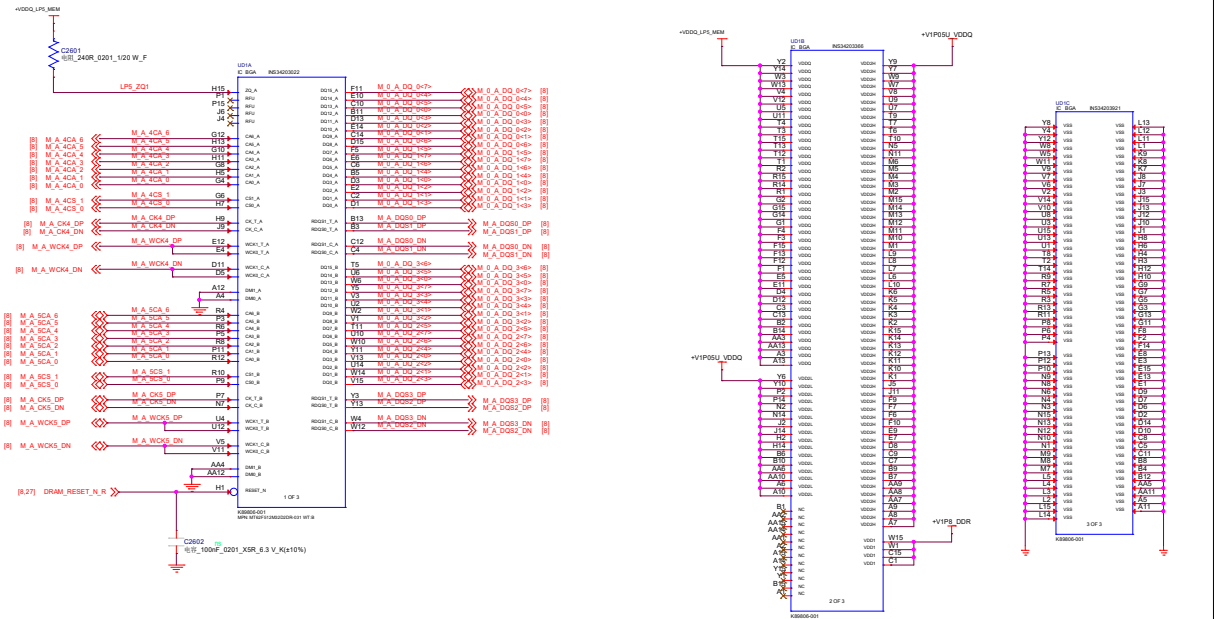
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4 caps per DRAM, 2 per edge close to VDDQ  
BGA's

MEMO\_LB5\_MEM

C3101 @10\_47uF\_0402\_XSR, 6.3 V, Mx20%

C3102 @10\_1uF\_0201\_XSR, 6.3 V, Mx20%

C3103 @10\_1uF\_0201\_XSR, 6.3 V, Mx20%

C3104 @10\_1uF\_0201\_XSR, 6.3 V, Mx20%

C3169 @10\_1uF\_0201\_XSR, 6.3 V, Mx20%

C3170 @10\_1uF\_0201\_XSR, 6.3 V, Mx20%

C3172 @10\_1uF\_0201\_XSR, 6.3 V, Mx20%

C3173 @10\_1uF\_0201\_XSR, 6.3 V, Mx20%

C3117 @10\_10uF\_0402\_XSR, 6.3 V, Mx20%

C3118 @10\_10uF\_0402\_XSR, 6.3 V, Mx20%

C3117 close to UD2601  
C3118 close to UD2701

VVP05U\_VDDQ

6 caps per DRAM, 2 per short edge and 1 per long edge close to VDD2H/VDD2L BGA's

C3145 close to UD2601  
C3146 close to UD2701

4 caps per DRAM, 2 per long edge close to VDD1 BGA's

C3149 (0/0, 1uF, 0201\_XSR, 6.3 V, Mx20%)

C3150 (0/0, 1uF, 0201\_XSR, 6.3 V, Mx20%)

C3151 (0/0, 1uF, 0201\_XSR, 6.3 V, Mx20%)

C3152 (0/0, 1uF, 0201\_XSR, 6.3 V, Mx20%)

C3153 (0/0, 1uF, 0201\_XSR, 6.3 V, Mx20%)

C3154 (0/0, 1uF, 0201\_XSR, 6.3 V, Mx20%)

C3155 (0/0, 1uF, 0201\_XSR, 6.3 V, Mx20%)

C3156 (0/0, 1uF, 0201\_XSR, 6.3 V, Mx20%)

C3174 (0/0, 10uF, 0402\_XSR, 6.3 V, Mx20%)

C3175 (0/0, 10uF, 0402\_XSR, 6.3 V, Mx20%)


C3174 close to UD2601

C3175 close to UD2701

+VDD1\_DDR

+VDD1\_VDDQ

+V1P05U\_VDDQ & +V1P8\_DDR discharge schematic

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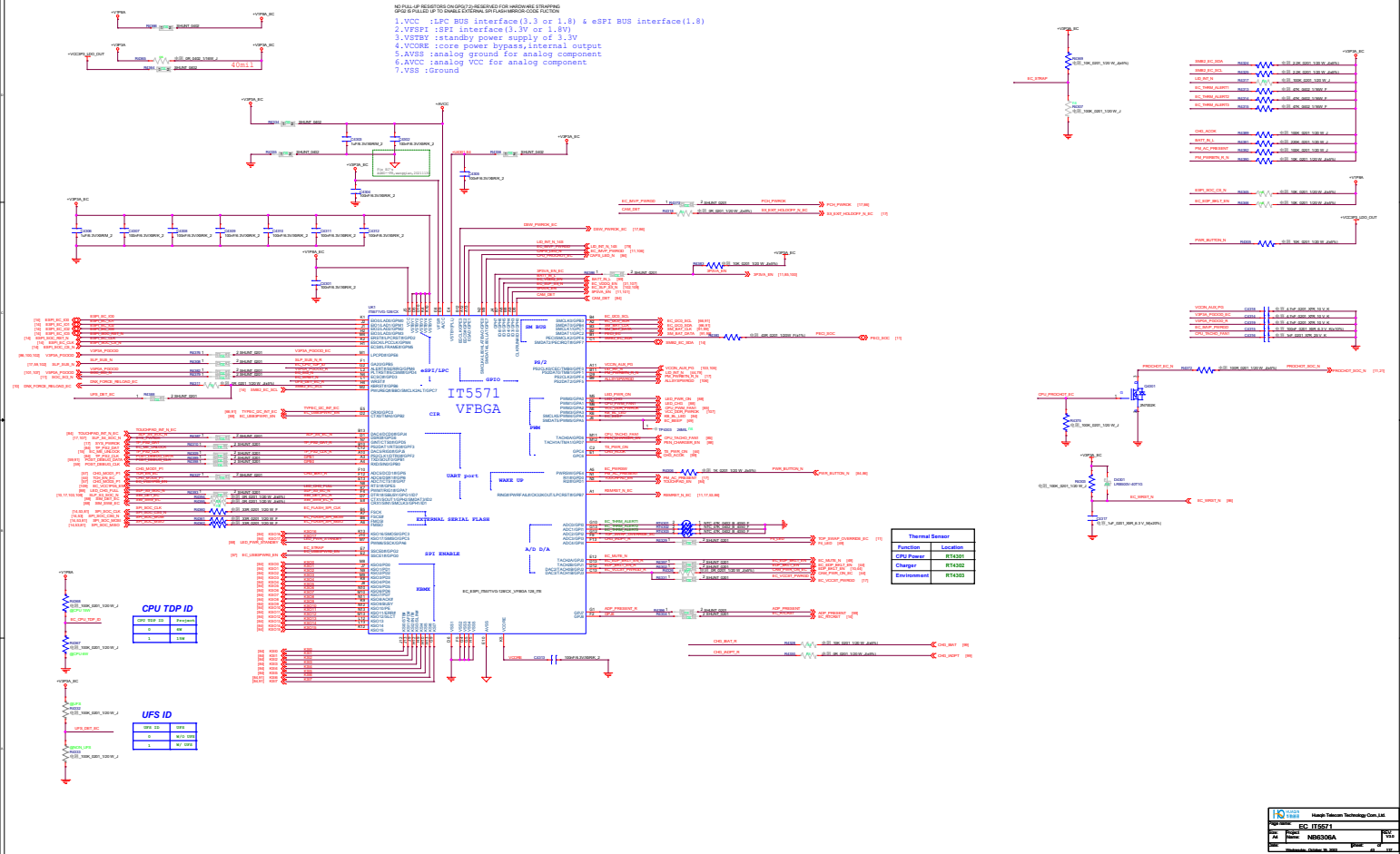
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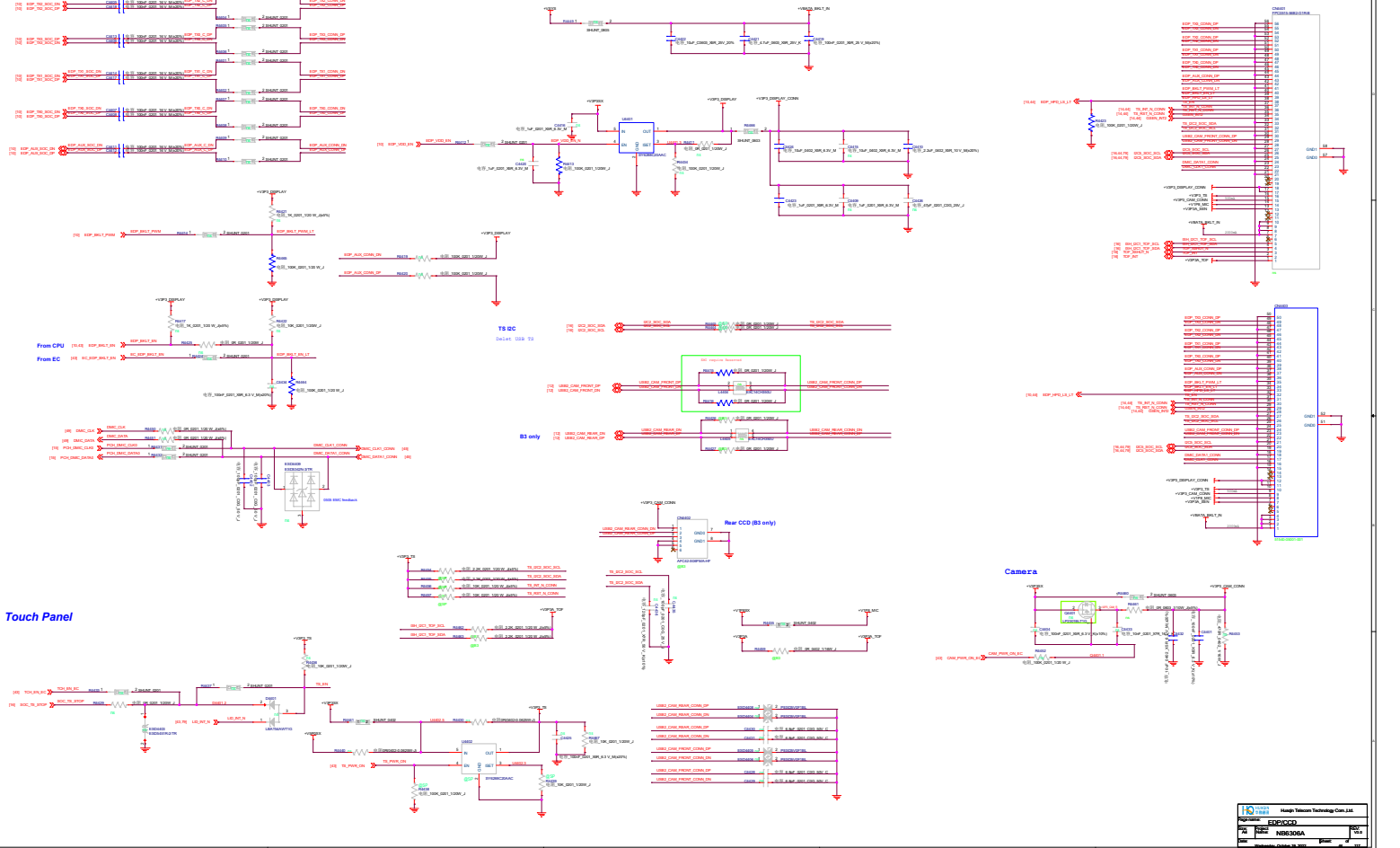
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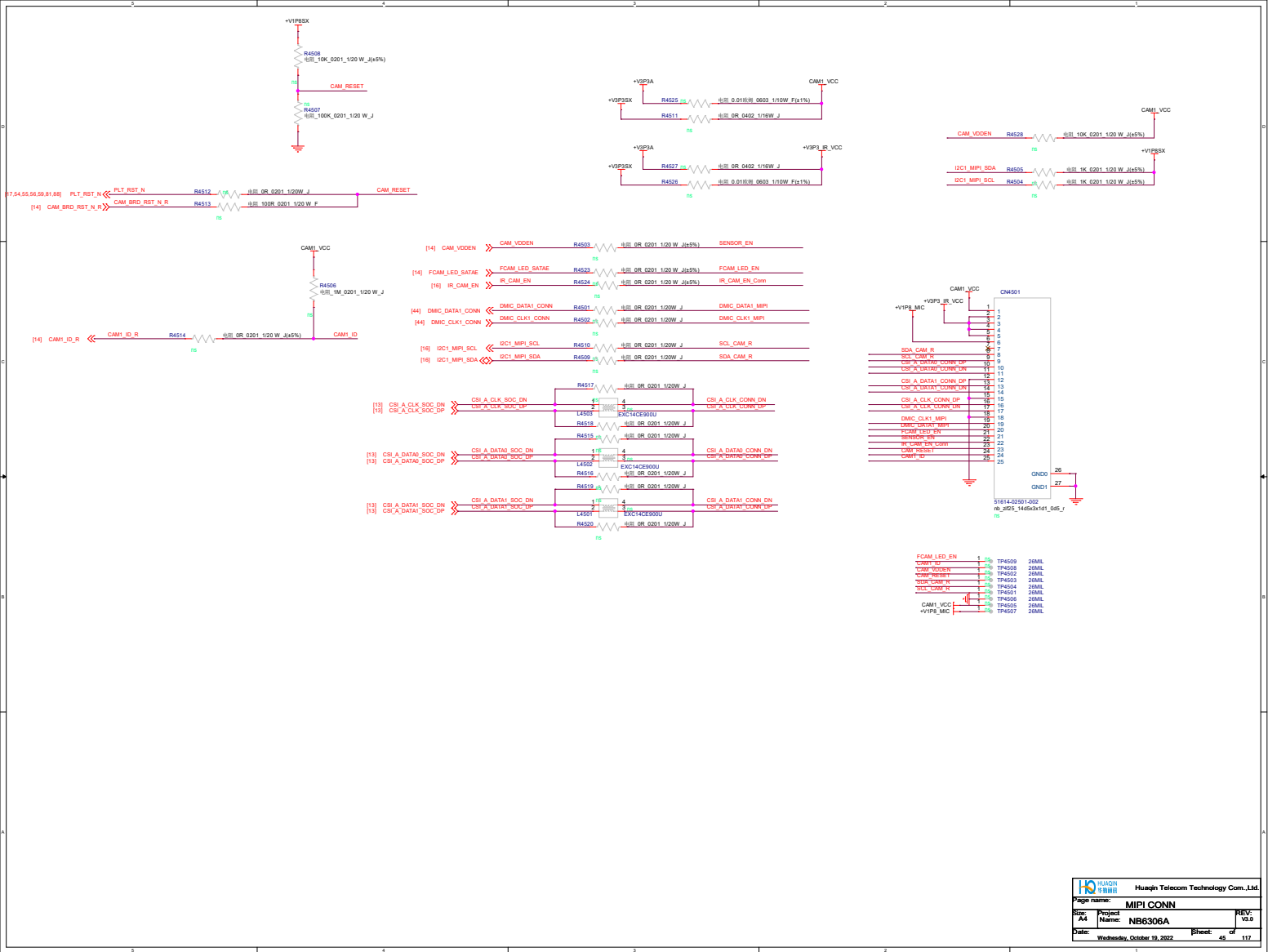
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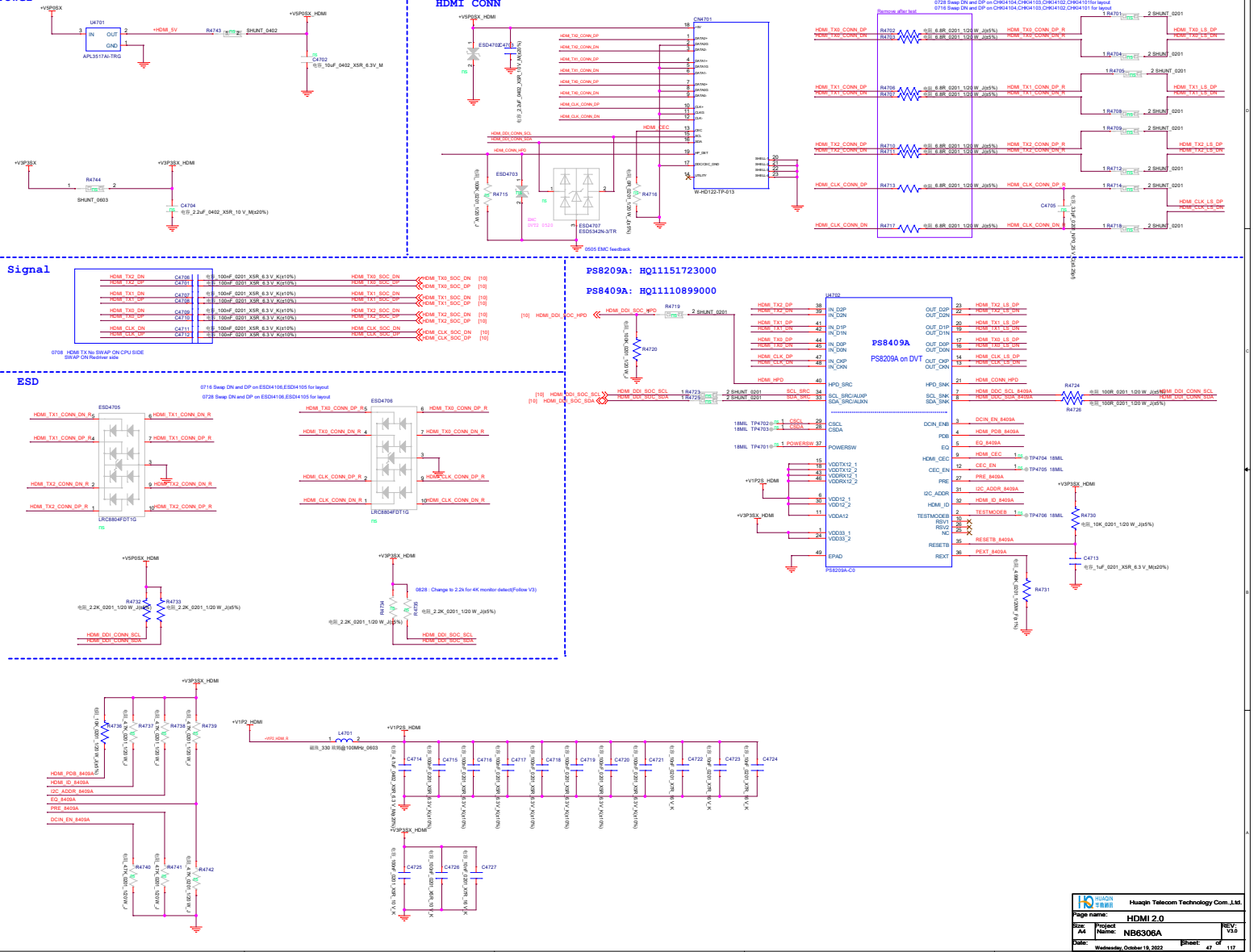







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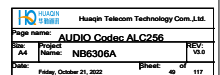


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+3.3V 1.8V DVDD	+3.3V 1.8V DVDD IO	Result
3.3V $\pm$ 10%	3.3V $\pm$ 10%	support
3.3V $\pm$ 10%	1.8V $\pm$ 5%	support
1.8V $\pm$ 5%	1.8V $\pm$ 5%	support
1.8V $\pm$ 5%	1.5V $\pm$ 5%	support
1.8V $\pm$ 5%	3.3V $\pm$ 10%	Not support





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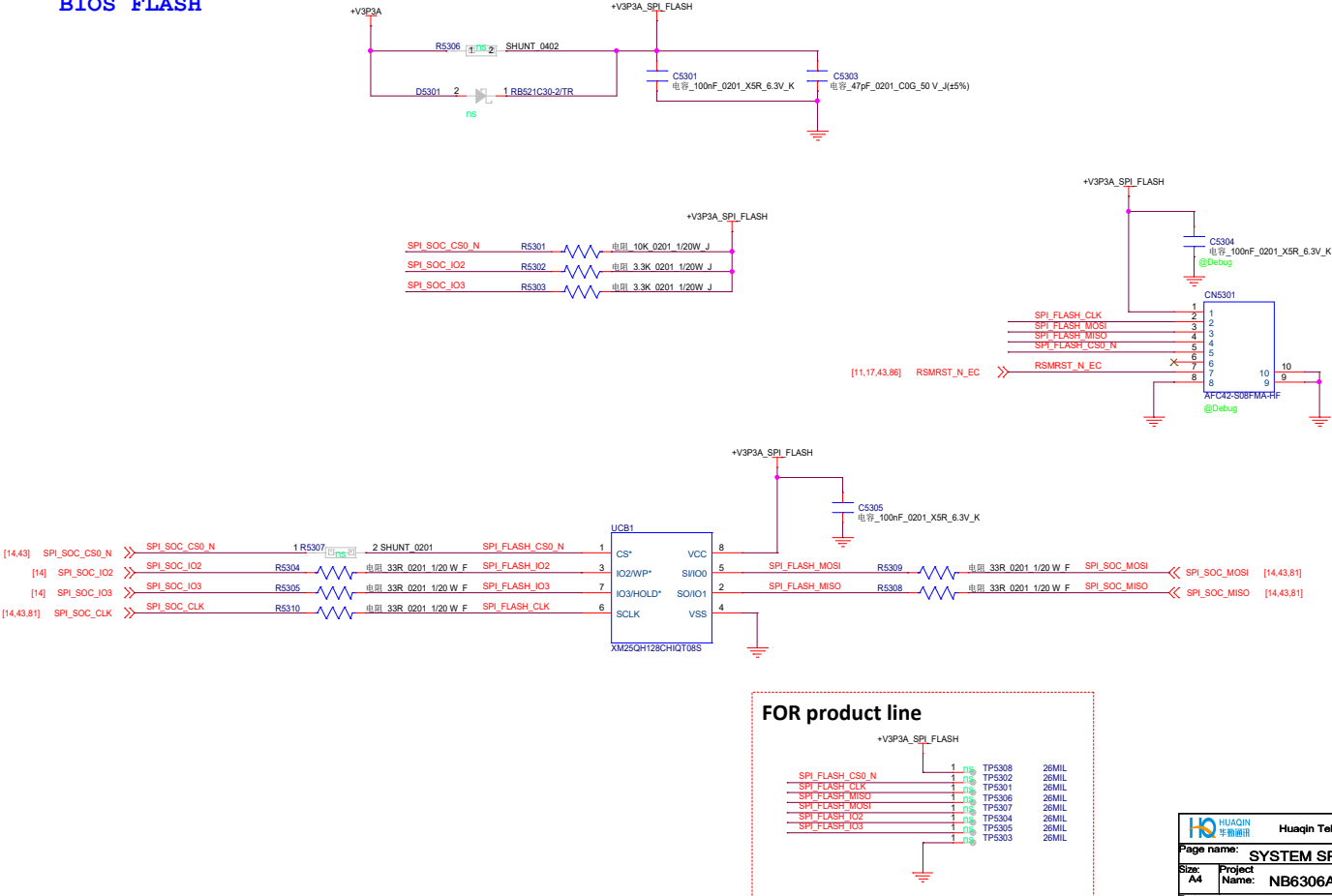
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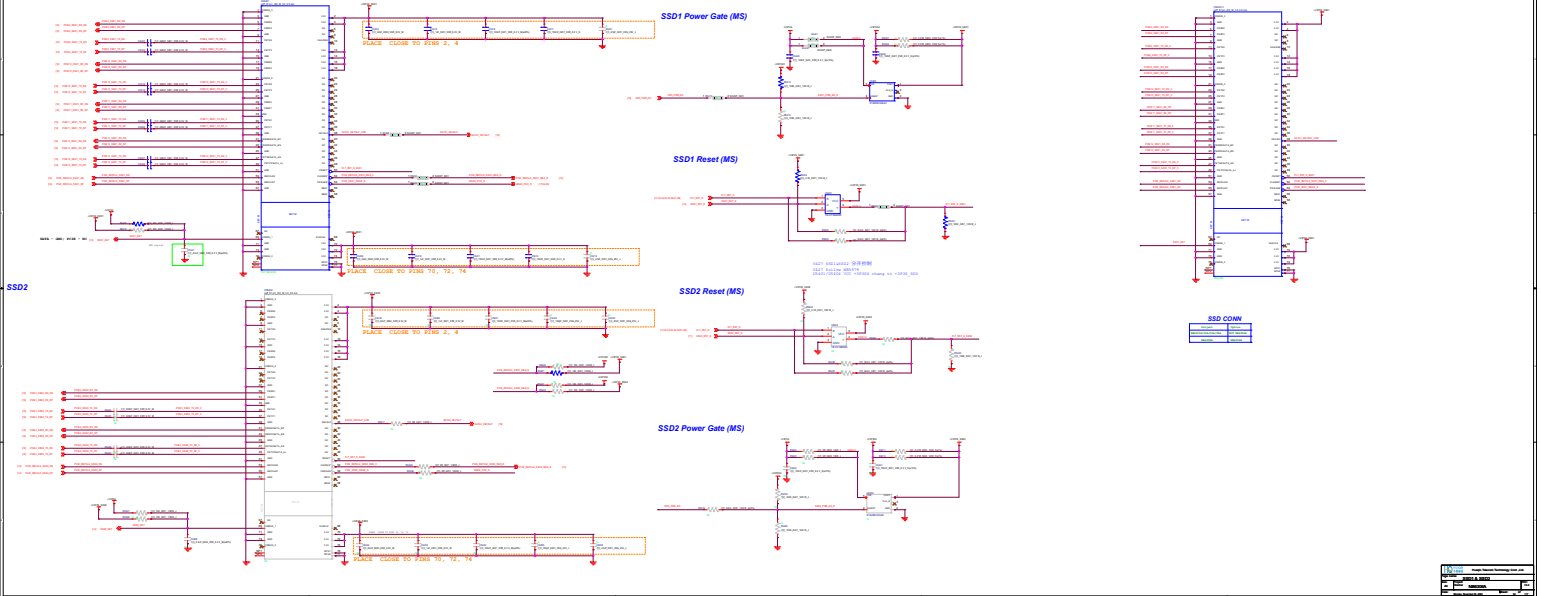
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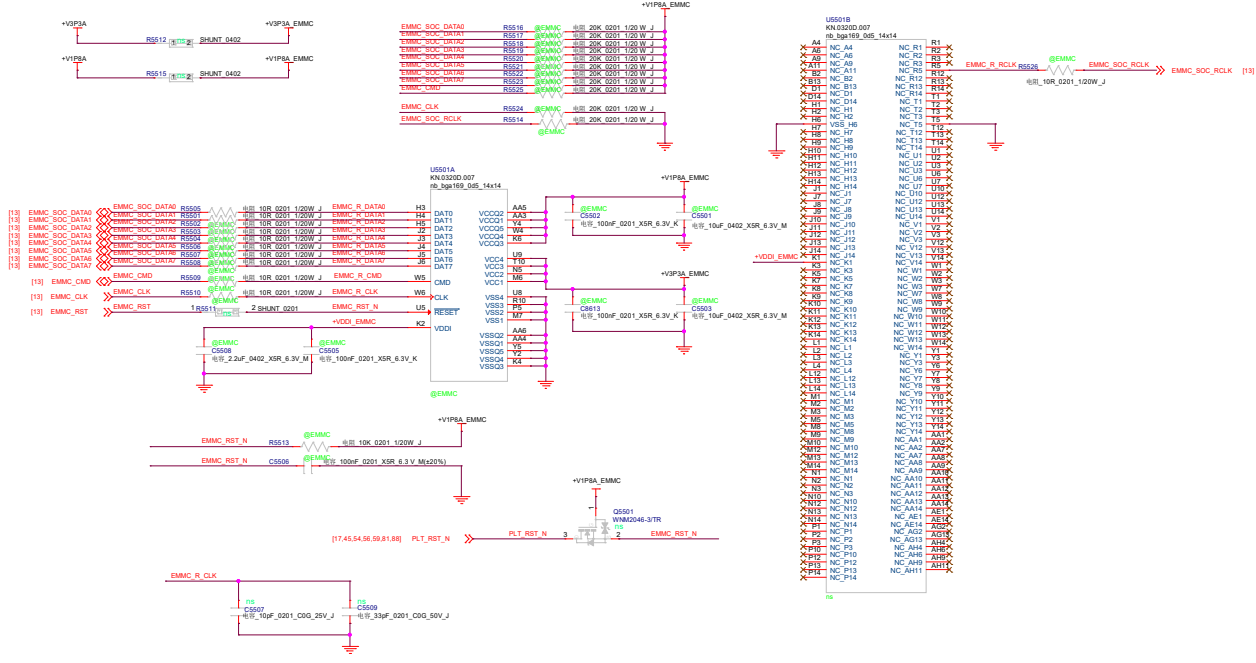
BIOS FLASH



SSD1

SSD2

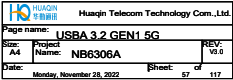








### USB3.2 AOU POWER(B3)





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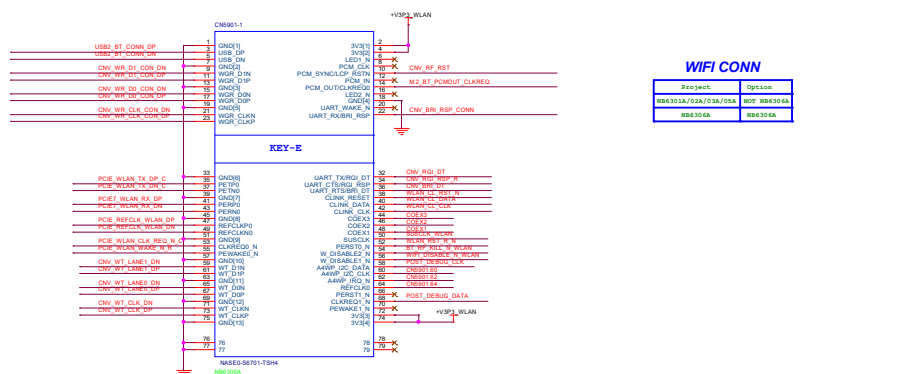
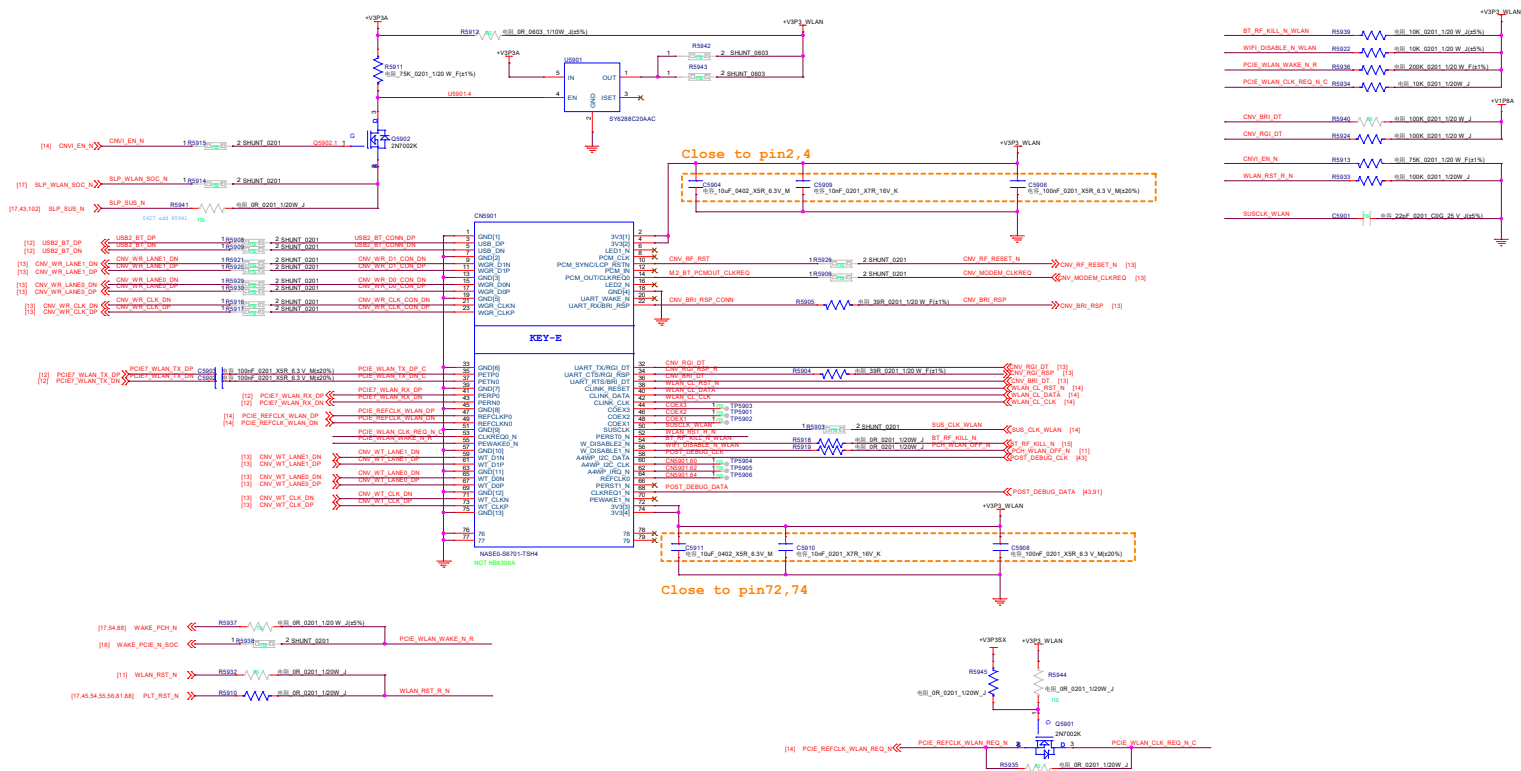
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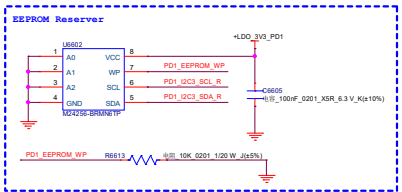
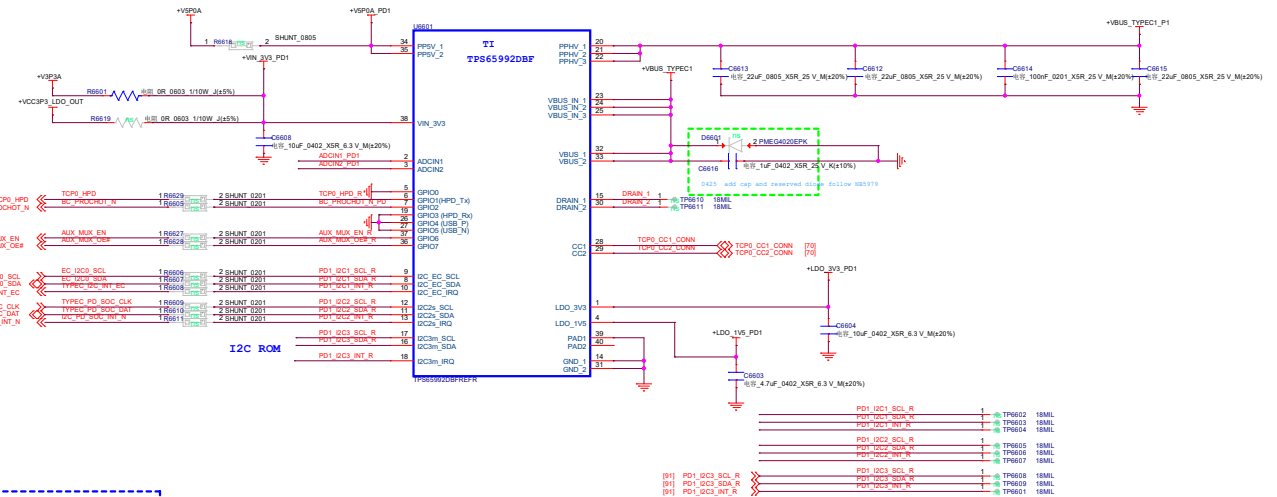
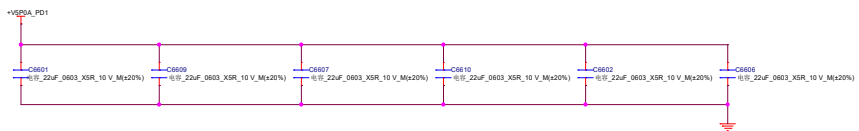
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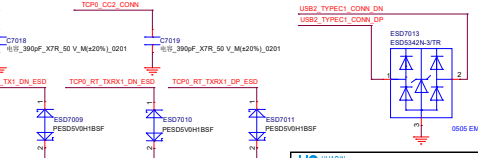
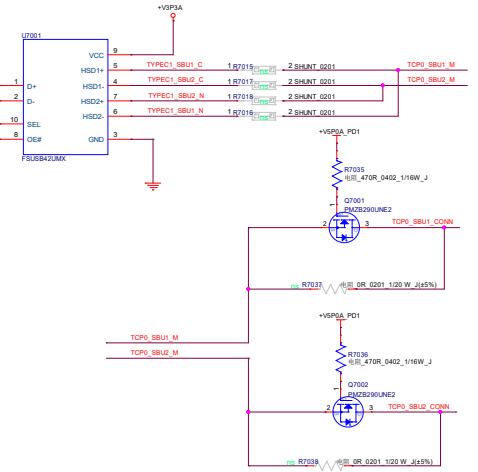
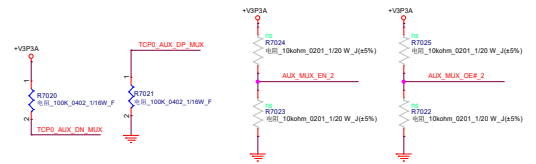
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# FUNCTION TABLE

OE	S	HSD1+, HSD1-	HSD2+, HSD2-
0	0	ON	OFF
0	1	OFF	OFF
1	x	OFF	OFF

Switches Shown For Logic "0" Input





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D

D

C

C

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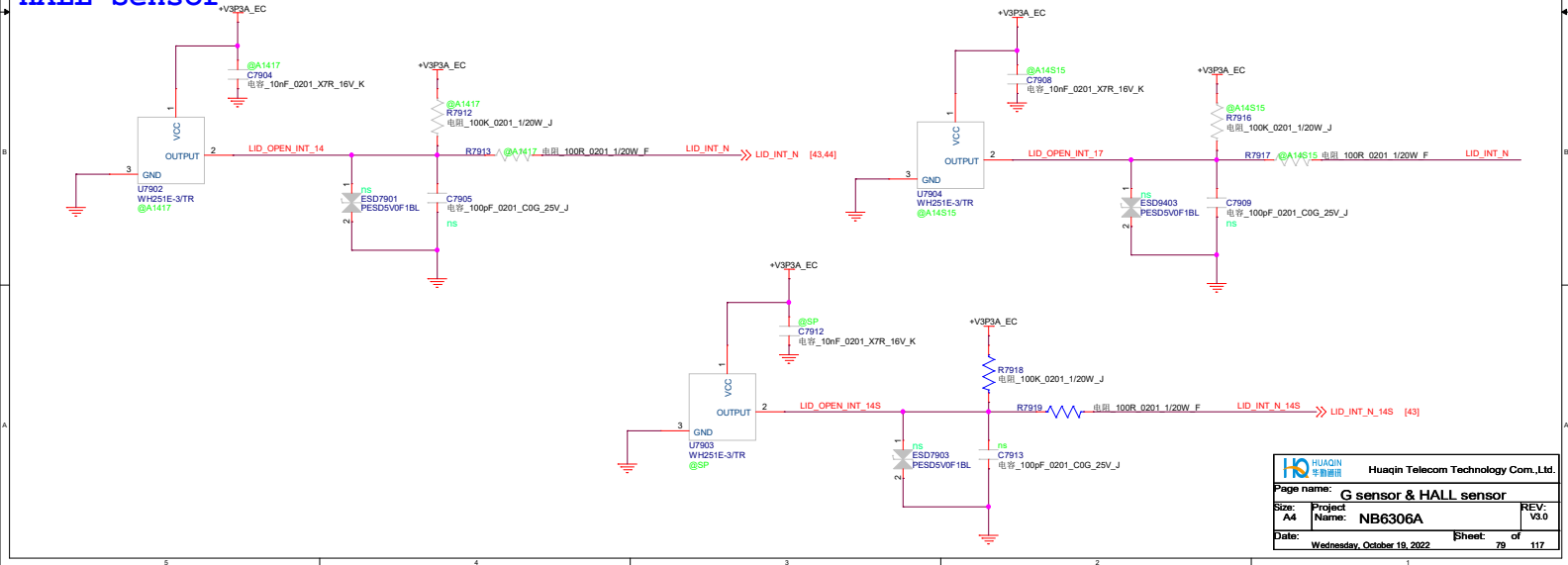
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## HALL Sensor





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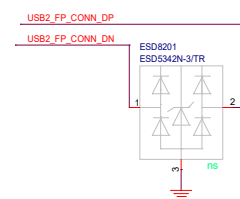
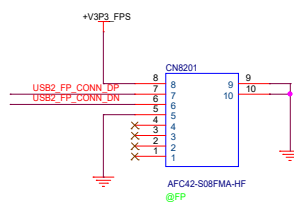
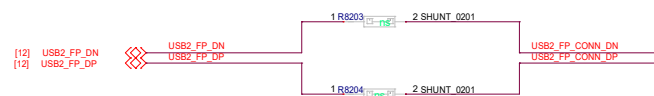
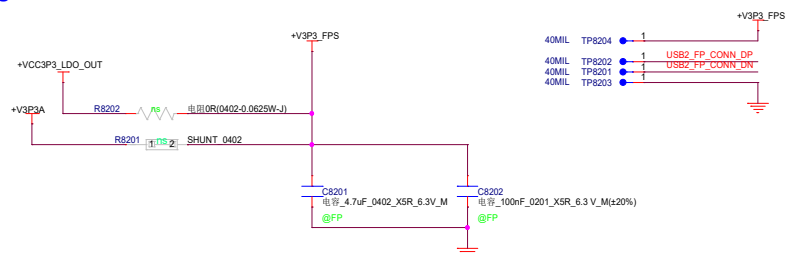



D

C

# B

A



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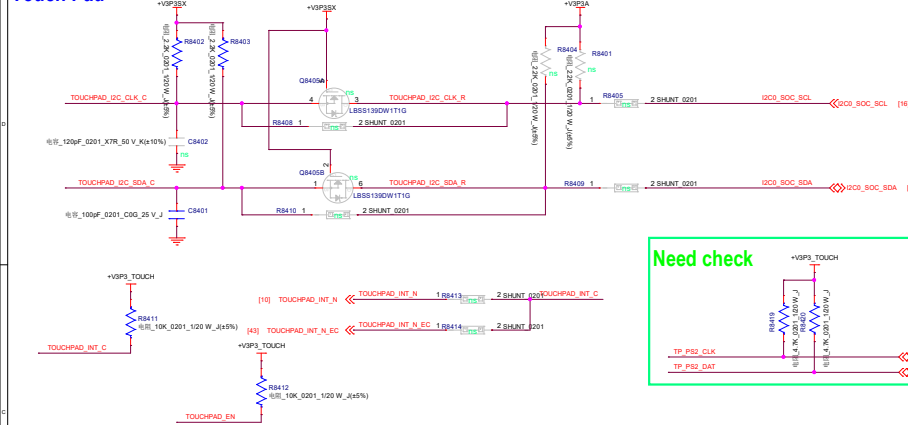
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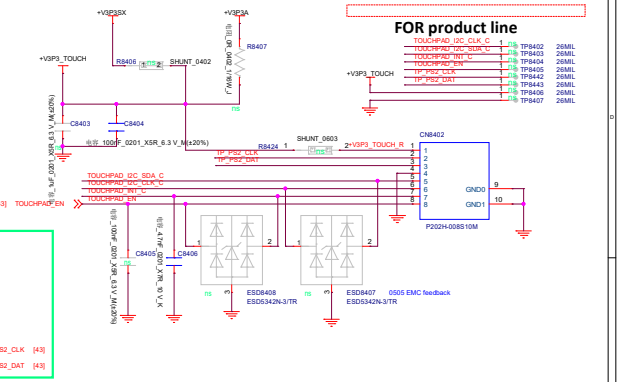
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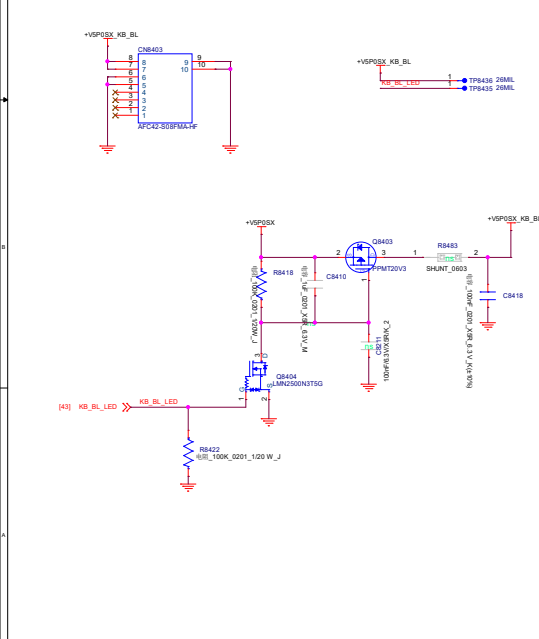
# Touch Pad



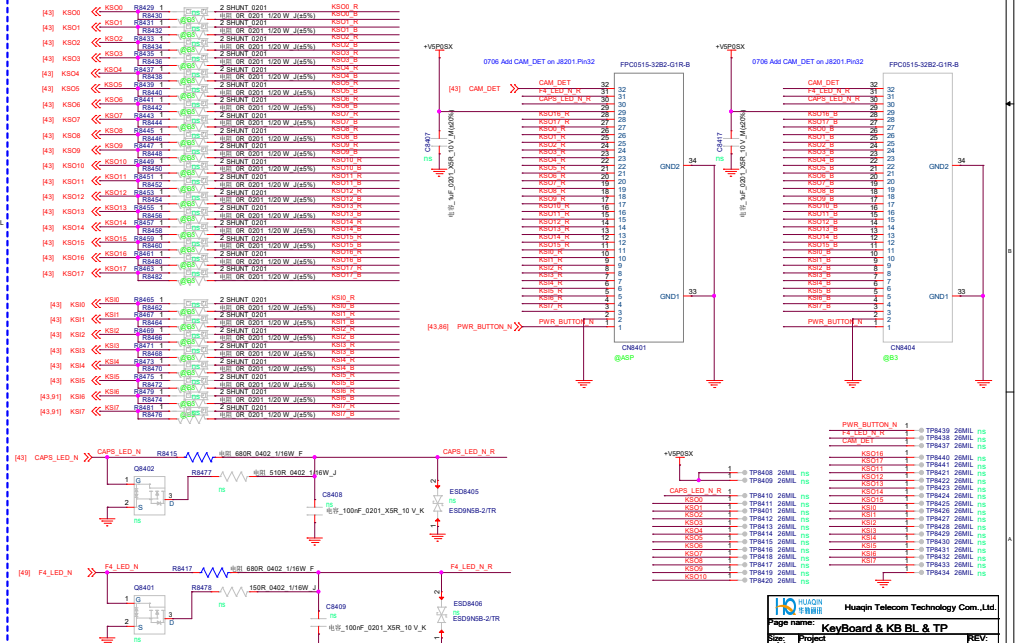
# Touch Pad CONN

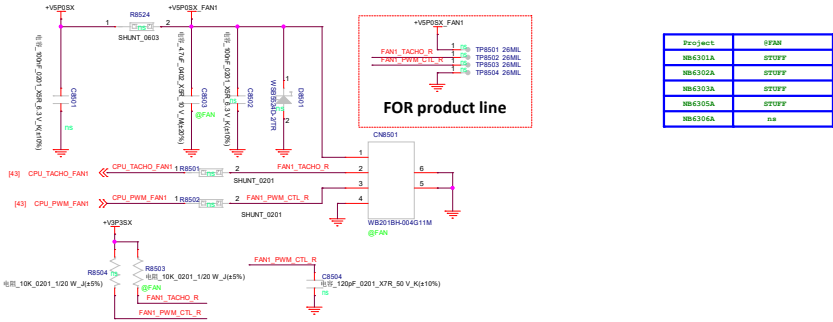


# KB Backlight

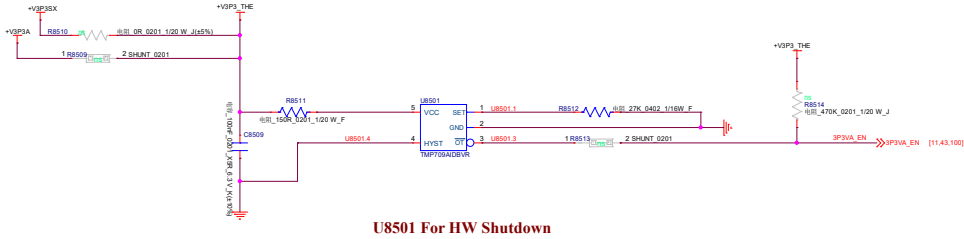


# KB CONN

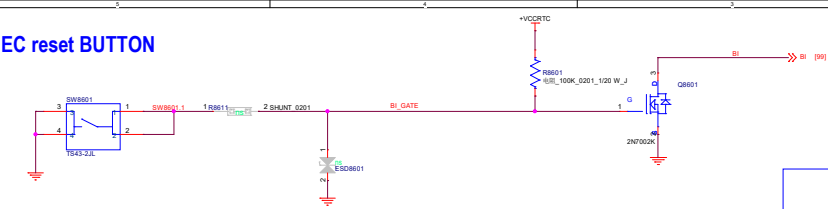




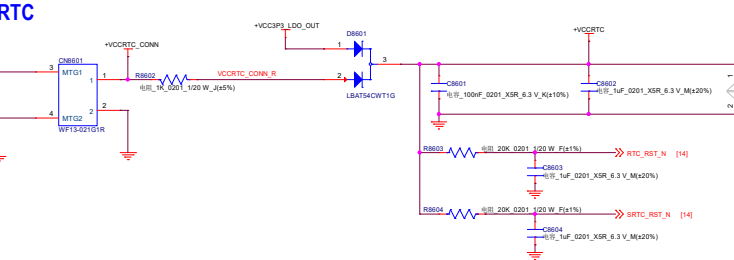
Thermal Sensor: HW



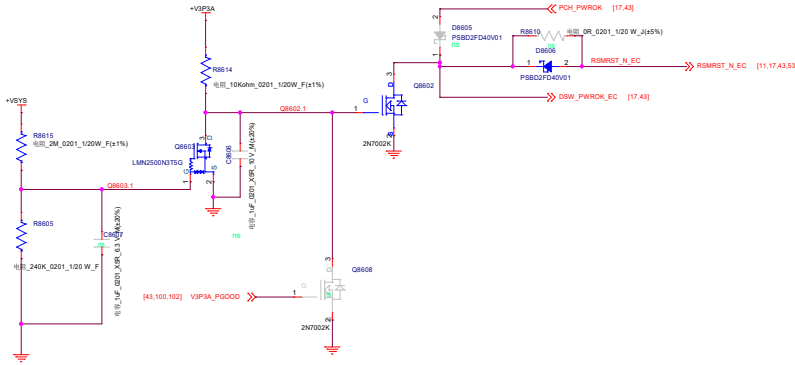
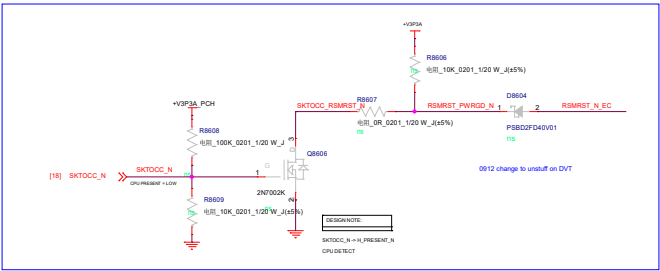
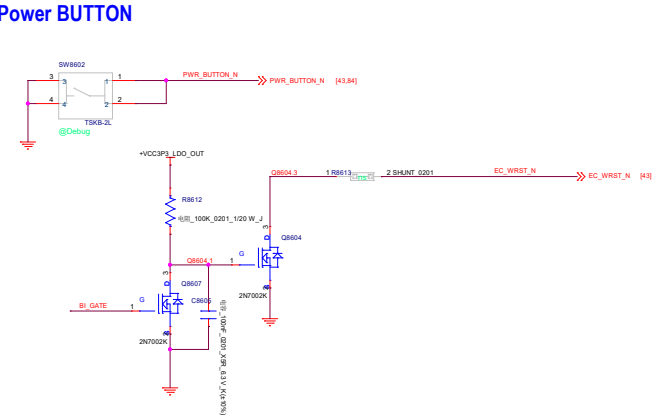
EC reset BUTTON



RTC



Power BUTTON





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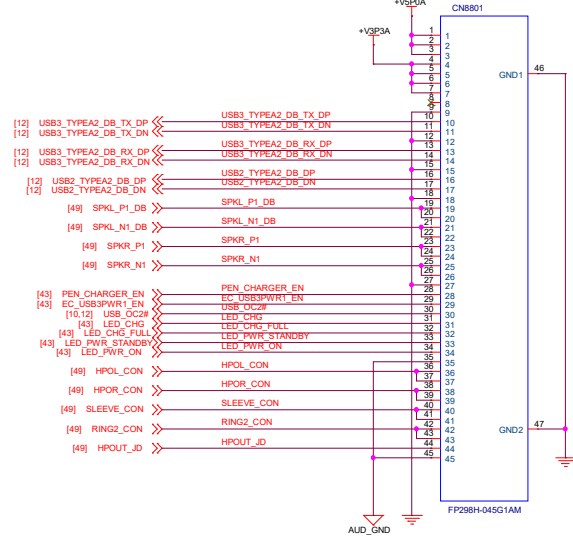
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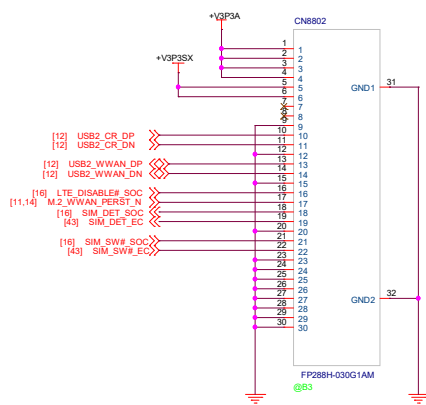
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DB & LTE CONN. & RJ45 CONN.

DB CONN.



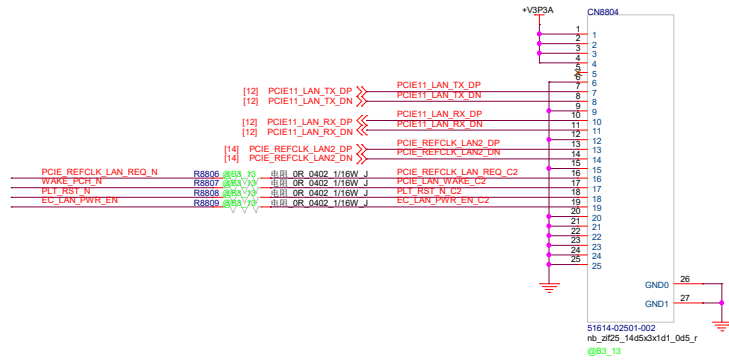
LTE CONN.



B3 11.6" LAN CONN.



B3 13" LAN CONN.







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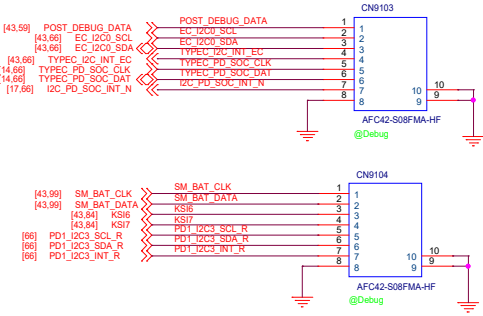
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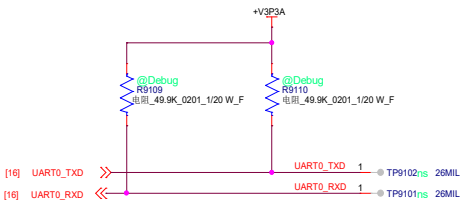
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PD\_FW FLASH AND I2C



System\_UART\_Debug





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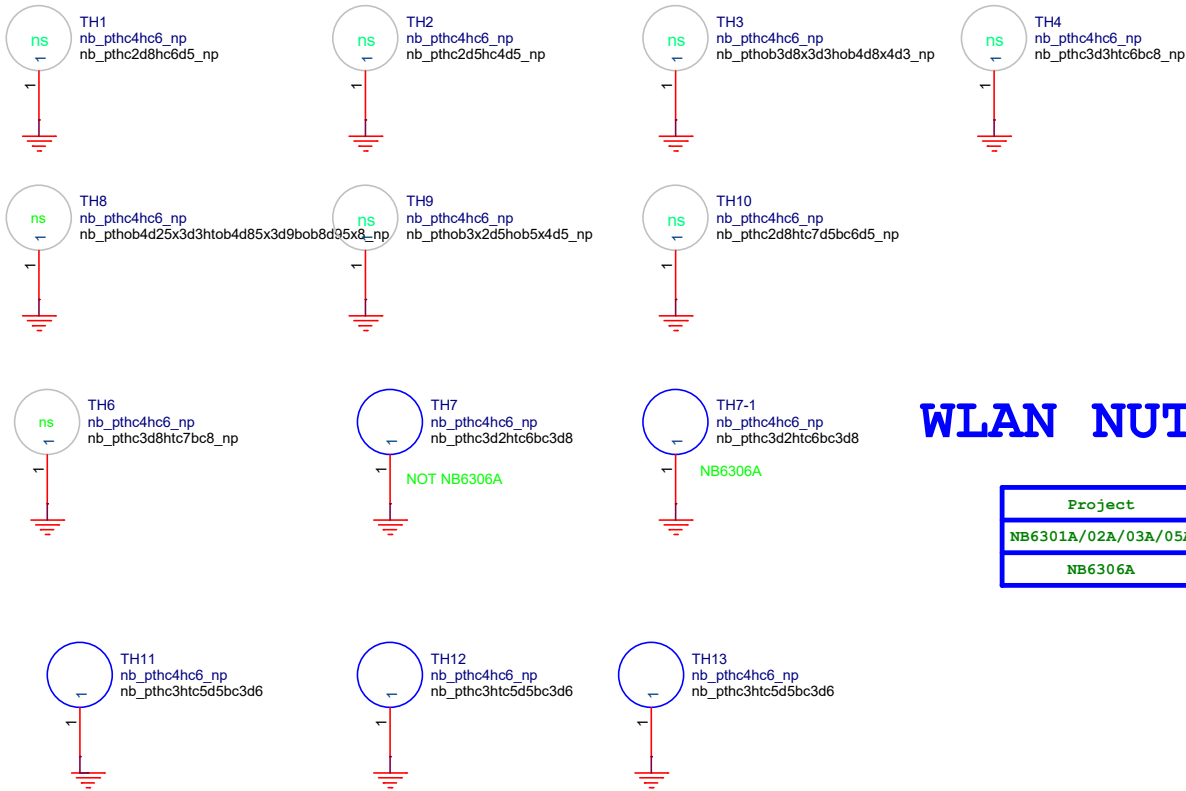
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# Hole



## WLAN NUT FOR TH7

Project	Option
NB6301A/02A/03A/05A	NOT NB6306A
NB6306A	NB6306A

## CPU NUT FOR TH11~TH13

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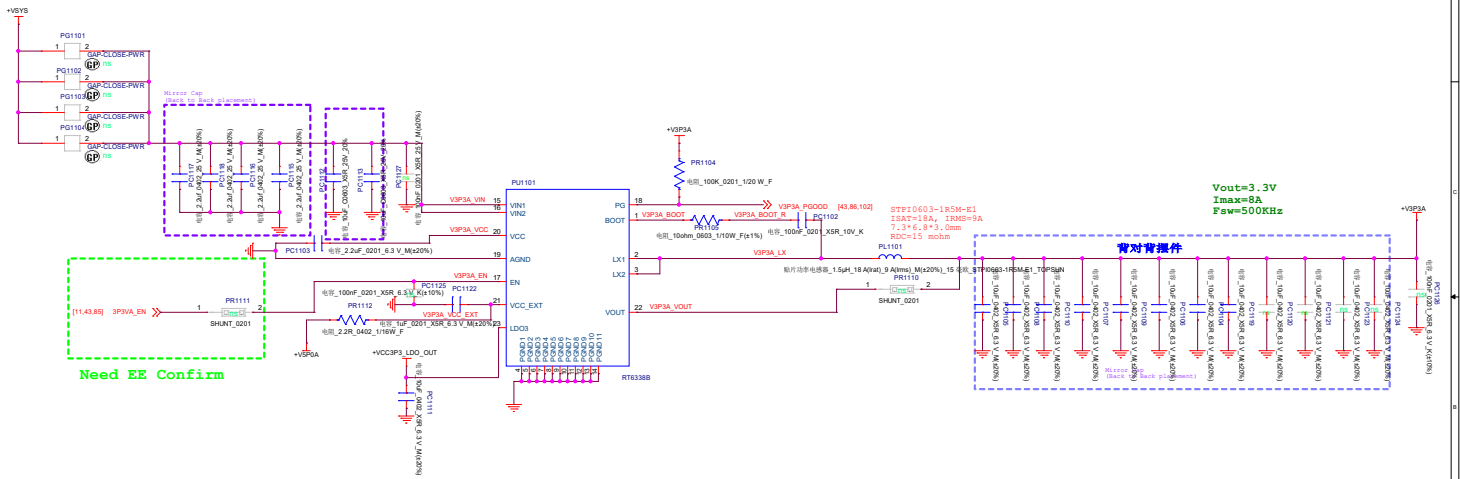
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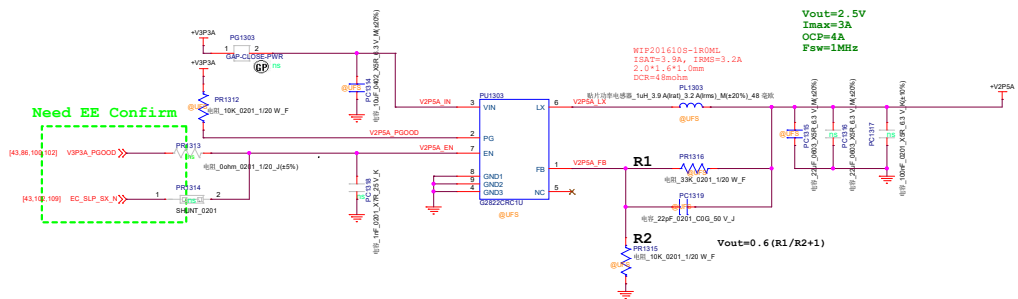
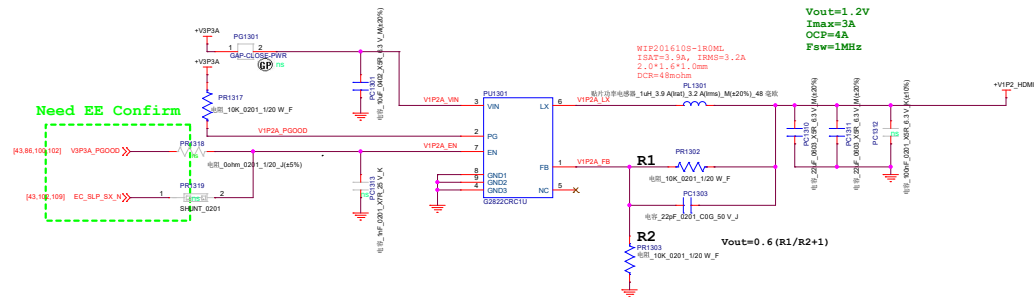
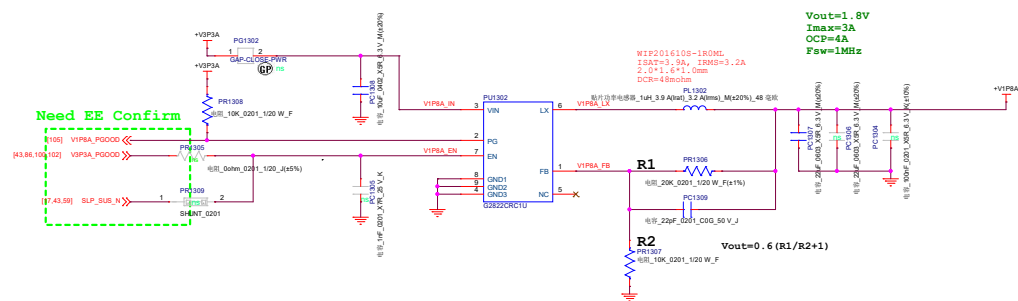
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# Change 0414







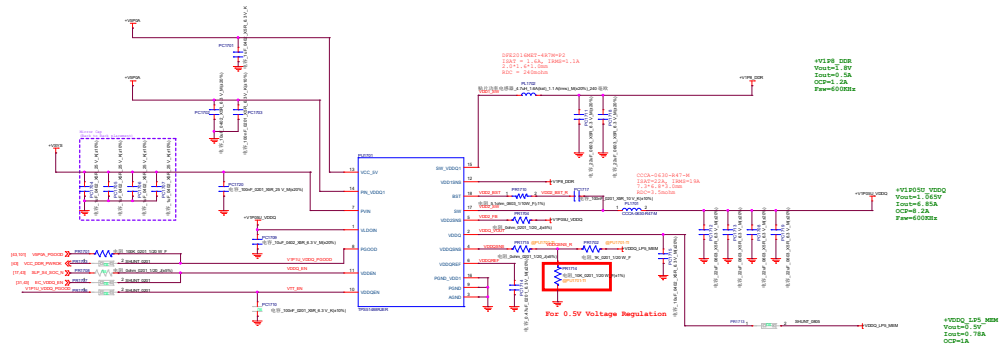






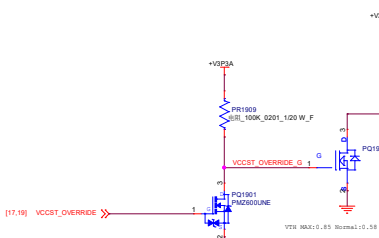




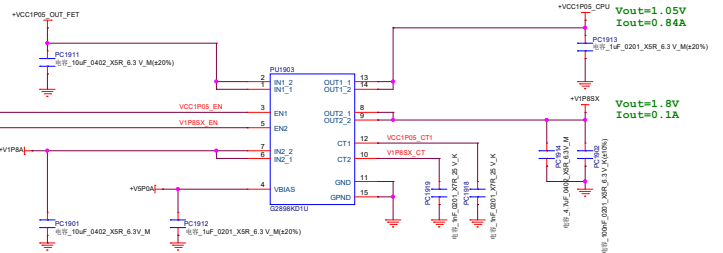
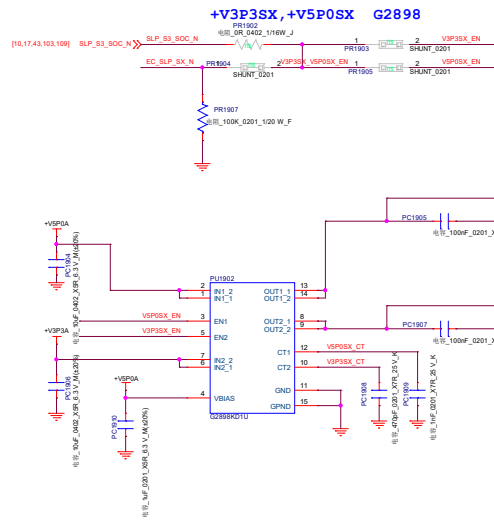
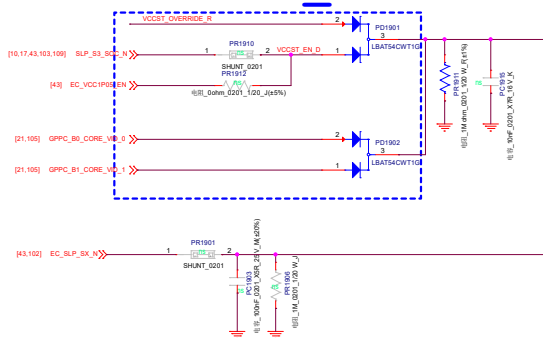


State	VDD1_0V1	VDD1_0V2	VDD1_0V3	VDD1_0V4	VDD1_0V5
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02	1	1	1	1	1
03	1	1	1	1	1
04	1	1	1	1	1
05	1	1	1	1	1
06	1	1	1	1	1
07	1	1	1	1	1
08	1	1	1	1	1
09	1	1	1	1	1
10	1	1	1	1	1
11	1	1	1	1	1
12	1	1	1	1	1
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## +VCC1P05\_CPU





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